IN THE SPECIFICATION:

Please amend paragraph number **[0004]** as follows:

[0004] A representative example of a known multi-chip module semiconductor ~~apparatus~~ device 10, prior to packaging, is shown in drawing FIG. 1.

Please amend paragraph number **[0005]** as follows:

[0005] A plurality of chips or dice 12A, 12B and 12C are mounted in a pyramidal stack on a substrate 14. Each die is mounted with an adhesive material 16 to the next lower die or substrate and is electrically connected to the ~~metallized~~ metalized substrate 14 by bond wires 18 using known wire bonding methods. Variants of this multi-chip configuration are described in United States Patent 5,422,435 to Takiar et al., Japan Patent 62-8534(A) to Tsukahara and Japan Patent 3-165550(A) to Yashiro. In each of these references, a pyramidal stack is formed of increasingly smaller chips or dice 12, in order to accommodate the placement of bond wires 18 on peripheral portions of each die 12. This configuration is not generally useful where dice of equal dimensions are to be placed in a multi-chip module (MCM), such as in a memory device.

Please amend paragraph number **[0006]** as follows:

[0006] In drawing FIG. 2, a pyramidal stack of chips in device 10 is shown as described in United States Patent 5,399,898 to Rostoker. In these references, the ~~dice12A,~~ dice 12A, 12B, 12C comprise "flip-chips" with solder bumps or balls 20 joined to conductive areas on the ~~backside~~ back side 22 of the underlying chip.

Please amend paragraph number **[0007]** as follows:

[0007] Depicted in drawing FIG. 3 is ~~a MCM configuration~~ an MCM device 10 in which a first die 12A is attached to a substrate 14 with adhesive 16 and is electrically connected to the substrate 14 with bond wires 18. A second die 12B is stacked atop the first die 12A and connected to it by solder balls 20. The second die 12B is smaller than the first die 12A, in order to leave access to the first die's 12A conductive areas. This type of arrangement is depicted in

Japan Patent ~~56-158467(A)~~ 56-158467(A) to Tsubouchi, and a variant thereof is described in Japan Patent 63-104343 to Kuranaga.

Please amend paragraph number **[0010]** as follows:

[0010] There have been various configurations of MCM ~~packages~~ devices in which chips of equal dimensions are stacked. Several such configurations are shown in drawing FIGS. 5, 6, 7, 8, 9, 10 and 11 and described below.

Please amend paragraph number **[0011]** as follows:

[0011] In one MCM device configuration shown in United States Patent 5,973,403 to Wark and Japan Patent 5-13665(A) to Yamauchi, a flip-chip 12A is electrically bonded to a substrate 14 by posts, balls or other connectors 20, and a second chip, i.e., die 12B, is attached back-to-back to the flip-chip 12A (with an intervening insulation layer 24) and connected by wires 18 to the substrate 14. This particular MCM device 10 is illustrated in drawing FIG. 5.

Please amend paragraph number **[0013]** as follows:

[0013] An MCM ~~apparatus~~ device 10 which combines various die configurations already described above in drawing FIGS. 1 through 6 is shown in United States Patent 6,051,878 to Akram et al. The apparatus uses conductive column-like structures to connect substrates which carry the dice.

Please amend paragraph number **[0014]** as follows:

[0014] As shown in drawing FIG. 7, an MCM device 10 described in United States Patent 5,483,024 to Russell et al. has two identical dice 12A, 12B with central bond pads. The dice are sandwiched between and attached to two lead frames 14A, 14B with discontinuous adhesive layers 16A and 16B. The dice 12A, 12B are joined by an intervening insulation layer 24. Bond wires 18 connect each die to the corresponding lead frame.

Please amend paragraph number **[0016]** as follows:

[0016] Described in United States Patent 5,291,061 to Ball is a similar stacked device 10 in which the thickness of the adhesive layers 16A, 16B and 16C is reduced, using a ~~low-loop-profile~~ low-loop-profile wire-bonding operation.

Please amend paragraph number **[0017]** as follows:

[0017] As shown in drawing FIG. 9, a device configuration generally shown in United States Patent 5,399,898 to Rostoker uses an upper flip-chip die 12E to join dice 12A mounted on a substrate 14. The dice 12A are connected to substrate metallization with bond wires 18. Thus, the ~~apparatus~~ device 10 comprises three dice connected serially.

Please amend paragraph number **[0018]** as follows:

[0018] There are various forms of ~~a MCM apparatus~~ an MCM device in which separate enclosed units are first formed and then stacked. Examples are described in United States Patent 5,434,745 to Shokrgozar et al. and United States Patent 5,128,831 to Fox, III et al. A typical stacked ~~apparatus~~ device 10 of this construction is depicted in drawing FIG. 10, showing three units. Each unit comprises an intermediate substrate ~~14A~~ 15A with a ~~metallized~~ metalized surface. A die 12A, 12B or 12C is mounted on the intermediate substrate ~~14A~~ 15A and connected to the metallization 30 by bond wires 18. A wall 32 surrounding each die 12 encloses the die 12, bond wires 18, and metallization 30. The various metallization leads extend to conductive columns 34 within the wall 32, the latter connected to metallization 40 on substrate 14. An insulative cover 38 protects the upper unit and forms a protective shell about the device.

Please amend paragraph number **[0019]** as follows:

[0019] In another design of MCM package ~~design~~ device 10 shown in drawing FIG. 11, a plurality of dice 12A, 12B, . . . have ~~bevelled~~ beveled edges 28 which permit the bonding of wires to edge bond pads on the active surfaces 26. This design requires that the die

thickness 36 be sufficiently great to accommodate wire loop height in the ~~bevelled~~ beveled regions. If the die thickness 36 is insufficient, the thickness of adhesive layers 16 must be increased. Thus, the device height will be increased. Also, the ~~bevelled~~ beveled edges 28 are weak and subject to breakage.

Please amend paragraph number **[0020]** as follows:

[0020] In each of the above prior art configurations for forming MCM ~~packages~~ devices containing a stack of identically configured dice, various limitations and/or problems exist as indicated above. A new ~~package~~ device design is needed in which a plurality of identical dice with bond pads along one edge or two edges may be readily stacked for parallel operation. The new design must provide a ~~package~~ device requiring fewer manufacturing steps and providing high density with enhanced reliability.

Please amend paragraph number **[0023]** as follows:

[0023] The substrate may be any body which supports the device, including for example, a circuit board, circuit card such as a multiple memory card, a lead frame or a tape automated bonding (TAB) tape. The bond pads of each die are exposed for rapid precise bond wiring to the substrate. In one embodiment, the apparatus is formed as a single stack of dice connected to a substrate whose reverse surface is configured for solder-ball bonding to another ~~metallized~~ metalized surface.

Please amend paragraph number **[0025]** as follows:

[0025] Where the stack comprises more than two semiconductor dice, the offset of each semiconductor die may be positive or negative along both axes. The stack may include a reversal in the direction of offset. In this case, the die underlying the die having an offset direction change must also be rotated in orientation about a central Z-axis. The active surface of the semiconductor die may be rotated to place the bond pads adjacent a different location of the

substrate. Such rotation may comprise 0, 90, 180 or 270 degrees in a clockwise or ~~counter-clockwise~~ counter-clockwise direction.

Please amend paragraph number **[0029]** as follows:

[0029] FIGS. 1 through 11 are side views of various prior art configurations of ~~multi-chip modules~~ multi-chip module (MCM) devices;

Please amend paragraph number **[0052]** as follows:

[0052] A new stacked multiple chip device formed of a plurality of offset Z-stacked, i.e., vertically-stacked semiconductor dice, together with a method of production thereof are provided by the invention. Some devices of the invention may be classified as stacked multi-chip modules (MCM). Semiconductor dice which are particularly usefully stacked in this construction are those having conductive bond pads along one edge, or alternatively along two adjacent edges of the active surface. In addition, a particular embodiment will be described which utilizes elongated, i.e., semiconductor dice having bond pads along opposing distal edges of a nonsquare elongated active surface. Although the device is particularly adapted to dice of the same surface dimensions and similar bond pad layout, a stack of dice may be formed in accordance with this invention which includes one or more semiconductor dice of a differing configuration at either end of the stack, or interposed therein. The stack of semiconductor dice is physically attached to a substrate, in which the substrate may comprise, for example, a printed circuit board (PCB), a memory card, a lead frame, tape automated bonding (TAB) tape or other substrate. Additionally, similar shaped dummy ~~die~~ dice of silicon and the like may be used as spacers between semiconductor ~~die~~ dice in the stack.

Please amend paragraph number **[0054]** as follows:

[0054] In this description, bond wires will be described as being connected between a semiconductor die and a substrate. It is to be understood that the wires are bonded to bond pads on the semiconductor die and to conductive members such as metallization or a lead frame which

may constitute all or part of the substrate. The device may also include semiconductor~~-die-to-semiconductor-~~ die-to-semiconductor die bonds.

Please amend paragraph number **[0056]** as follows:

[0056] Semiconductor die 60A is shown attached to a substrate 70 by adhesive layer 78. The adhesive layer 78 may be any adhesive capable of bonding a reverse surface 72 of a die 60 to the active surface 52 of another semiconductor die or to a~~-topside-~~ top side 66 of a substrate 70. Semiconductor die 60B is stacked on top of semiconductor die 60A and joined to it by thin adhesive layer 78. Semiconductor die 60B is offset from semiconductor die 60A along Y-axis 76 a distance 82 which exposes the field 55 of bond pads 54A. The offset distance 82 may be the shortest distance which permits reliable use of a wire bonding tool, not shown, to bond conductors such as bond wires 62 to the bond pads 54A. Thus, bond pads 54A, 54B are joined by fine metal bond wires 62 or other conductive members to conductive, e.g., metallization areas 58 on the~~-topside-~~ top side 66 of substrate 70. If so dictated by the design of the device 50, certain bond pads 54A and 54B may also be conductively connected to each other, i.e., on the same semiconductor die 60A or 60B, or from semiconductor die 60A to semiconductor die 60B.

Please amend paragraph number **[0061]** as follows:

[0061] A stack 61 of two or more offset semiconductor dice 60 may also be formed on a lead frame 94, as depicted in an example in drawing FIG. 12A. The lead frame 94 is typically formed from a material such as copper, copper alloys, iron-nickel alloys, or the like. Other materials, such as TAB tape, could be used in accordance with this invention as well. The lead frame 94 is shown with opposing runners 96, a central paddle 98, and leads 102A and 102B to which wires are attached. The lead frame 94 has alignment mechanisms 100 such as precisely positioned marks or holes, for precise positioning of the lead frame 94 during operations such as die bonding and wire bonding where alignment is critical. In this example, semiconductor die 60A is attached to a paddle 98 of lead frame 94 with a thin adhesive layer, not shown. The

paddle 98 serves as a substrate to support the stack 61. Semiconductor die 60B is then attached to overlie a major portion of semiconductor die 60A, wherein the die edge 56B along which bond pads 54 are positioned is offset a distance 82 from the die edge 56A of the lower semiconductor die 60A, to expose the bond pads 54. As shown, conductive bond wires 62A are connected from bond pads 54B of semiconductor die 60A to appropriate leads 102A. Likewise, bond wires 62B are connected from bond pads ~~56B~~ 54 to leads 102B. Alternatively, TAB bonding or other bonding methods may be used. As illustrated in drawing FIG. 12B, the semiconductor die 60B is of smaller size than that of semiconductor die 60A. Further, as illustrated in drawing FIG. 12C, the semiconductor die 60B is of larger size than semiconductor die 60A having three sides of the semiconductor die 60B overhanging the semiconductor die 60A.

Please amend paragraph number **[0062]** as follows:

[0062] In the embodiment of drawing FIGS. 12 through 14, both of the semiconductor dice 60A, 60B have their bond pads 54A, 54B oriented in the same direction so that they are connected by bond wires 62 to metallization areas 58 on the same side of the device 50. However, the semiconductor die orientation and other factors, such as semiconductor ~~die~~ dice having different sizes and dimensions, may be changed to suit a particular application. Thus, major design factors affecting the stacked offset multiple semiconductor die device 50 include the number of semiconductor dice 60 in the stack 61, die dimensions, number of die edges 56 along which bond pads 54 are arrayed, offset direction(s), offset distance 82 and rotation angle of each semiconductor die 60 relative to the semiconductor die 60 just below.

Please amend paragraph number **[0070]** as follows:

[0070] Illustrated in drawing FIGS. 19 and 20 are devices 50 which have a second semiconductor die 60B with a reverse offset and which is rotated 180 degrees relative to lowermost semiconductor die 60A. Semiconductor dice 60C and 60D are similarly rotated relative to semiconductor die 60A, and each is forwardly offset from its underlying die. In drawing FIG. 19, the bond wires 62 from the three upper semiconductor dice 60B, 60C and 60D

are bonded to the substrate 70 on the same side of the stack 61, while semiconductor die 60A is bonded on the opposing side of the stack. In drawing FIG. 20, semiconductor die 60D is attached to the stack 61 in an unrotated position relative to die 60A. Semiconductor die 60D has its bond wires 62D connected to substrate ~~14 in~~ 70 in the vicinity of bond wires 62A, i.e., on the opposite side of the stack from bond wires 62B and 62C.

Please amend paragraph number **[0071]** as follows:

[0071] As illustrated in drawing FIGS. 21 and 22, semiconductor dice 60B and 60C are offset in a reverse direction from semiconductor die 60A, and semiconductor die 60D is offset in a positive direction from underlying die 60C. Illustrated in drawing FIG. 21, semiconductor dice 60C and 60D are both rotated 180 degrees relative to semiconductor dice 60A and 60B, so that their bond pads 54C and 54D face in an opposite direction from bond pads 54A and 54B. Illustrated in drawing FIG. 22, semiconductor die 60D of the device 50 in drawing FIG. 21 has been rotated 180 degrees and ~~it's~~ its bond wires 62D attached to the substrate ~~14 in~~ 70 in the vicinity of bond wires 62A and 62B.

Please amend paragraph number **[0076]** as follows:

[0076] The stacked offset multiple die device 50 of this invention may have any form of substrate 70 known in the art. For example, the substrate 70 may be a ~~metallized~~ metalized lead frame as already shown in drawing FIG. 12A.

Please amend paragraph number **[0078]** as follows:

[0078] As shown in drawing FIG. 27, die 60B is offset in position in two directions. Thus, semiconductor die 60B is offset from semiconductor die 60A a distance 82A along the ~~X-axis~~ X-axis 74 and a distance 82B along the Y-axis 76, whereby all of the bond pads 54AA and 54AB of semiconductor die 60A are exposed for easy wire bonding.

Please amend paragraph number **[0080]** as follows:

[0080] A further embodiment of the invention is illustrated in drawing FIGS. 28 and 29, in which a semiconductor die stack 61 is formed of semiconductor dice 60 having bond pads 54 on each of two opposed edges 56 of the semiconductor die's active surface 52 (not shown). In this configuration, each added semiconductor die 60 is rotated 90 degrees or 270 degrees from the underlying semiconductor die to place the semiconductor die in an offset position. Each semiconductor die 60 has a length dimension 104 (not shown) which is longer than a width dimension 106 (not shown) by at least two times the required offset, i.e., to expose the bond pads 54 of the underlying semiconductor die. If desired, the semiconductor dice 60 can be of any convenient physical size and be of different physical size than the other. Use of more than two semiconductor dice 60 in the stack 61 results in semiconductor die bond pads 54 being overhung by a semiconductor die which is two positions higher in the stack. The manufacturing process will require intermediate wire bonding operations in this case. The stack configuration results in wire bonds 62A and 62C to metallization areas 58 of the substrate 70 on two opposing sides of the stack 61, and wire bonds 62B and 62D on the other two opposing sides of the stack. Thus, wire bonds are located on all four sides of the stack 61.

Please amend paragraph number **[0082]** as follows:

[0082] The various embodiments of stacked offset multiple semiconductor die devices which are shown and described herein are exemplary and not limiting. It is understood that other configurations may include additional elements, for example, such elements including additional semiconductor dice and lead frames, ~~heatsinks,~~ heat sinks, dielectric layers, packaging, etc., as known in the art.